REMARKS

Claims 108-110, 112, 114, 117-118, and 120 have been amended for clarity purposes. Claims 108-121 remain pending.

The Examiner has rejected claims 108-121 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Examiner asserts that the specification never discloses the dummy structure in the top conductive layer as claimed in claim 108. It is respectfully submitted that this language is supported on Page 5, Lines 16-17 (3rd line of the 3rd paragraph), among other places. The Examiner also recites that the specification never discloses a plurality of dummy structures used to facilitate an even polishing of a surface of the semiconductor as claimed in claim 108. This language is supported on the Last Line of Page 44 through the 1st Line of Page 44, among other places. The Examiner also asserts that the specification never discloses the voltage contrast structure is used to detect electrical defects as claimed in claim 108. This language is supported on Page 44, Line 9-12, among other places. The Examiner further recites that the specification never discloses the test structure comprises the first conductive layer, the first isolation layer, the second isolation layer, the first contact and the second contact as claimed in claim 110. This language is supported on Page 44, Line 6-9 and Fig. 24B, among other places.

The language of claim 111 is supported on Page 44, Line 10, among other places. The language of claim 112 and 113 are supported on Page 44, Lines 10-13, among other places. The Examiner asserts that the specification never discloses some of the test structures include contacts for coupling its dummy structure to a substrate of the semiconductor as claimed in claim 114. This language is supported on Page 44, Lines 6-9 and Fig. 24B and the last paragraph of Page 44, among other places. It is also asserted that the specification never discloses the claimed subject matter of claims 115 and 116. This language is supported on Page 44, Lines 10-12, among other places. The language of claims 117-121 is supported on Page 44, Lines 6-9, among other places.

The Examiner has rejected claims 114-116 under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner asserts that the phrase "forming a plurality of test structures on the semiconductor die, where at least a portion of each test structure includes a dummy structure" is vague and indefinite because claim 108 has disclosed the dummy test structures and the phrase is being repeated in claim 114. Claim 114 has been amended to clarify the invention.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a

telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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